IN THE CLAIMS:

Please amend the claims as follows:

1. (Cancelled)

2. (Previously presented) A digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form, comprising:

a circuit for establishing a synchronous signal in reception data based on a polarity of the most significant bit (MSB) of the reception transport packet data.

wherein the circuit for establishing the synchronous signal in reception data comprises:

a synchronous code pattern detecting circuit for detecting the segment synchronous code pattern from the most significant bit signal of the reception packet data,

a symbol number counter circuit for counting the number of symbol data in the reception packet data,

a synchronism detection establishing circuit for judging the true segment synchronous code pattern by obtaining the segment synchronous code pattern from said synchronous code pattern detecting circuit when said symbol number counter circuit finishes counting of a specified number, and

a synchronism detection protection counter circuit for detecting and establishing the segment synchronous signal in the reception data from the output of said synchronous code pattern detecting circuit and count-up of specified number of said symbol number counter circuit.

3. (Original) A digital broadcast demodulator of claim 2, wherein the most significant bit signal of the reception packet data is processed so as to issue a signal showing the start position of the synchronous signal in the data and a signal of detecting and establishing the synchronous signal.

4. (Cancelled)

5. (Previously presented) A digital broadcast demodulator of claim 2, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form,

wherein a differential value of synchronous signals of reception packet data is determined so as to detect a clock phase error of transmission data, and a clock signal is regenerated by phase control on the basis of said clock phase error,

said digital broadcast demodulator further comprising a clock phase error detecting circuit for issuing a clock phase error of transmission data by determining the difference of the N-th and N+1-th (N>1) synchronous signals which should be of same level by nature, from the code pattern detection signal of synchronous signal and signal showing position of synchronous signal.

6. (Currently amended) A digital broadcast demodulator, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form,

wherein a differential value of synchronous signals of reception packet data, which should be of the same level by nature, is determined so as to detect a clock phase error of transmission data, and a clock signal is regenerated by phase control on the basis of said clock phase error,

said digital broadcast demodulator further comprising:

(a) a subtracting circuit for subtracting the N-th input from the N+1th input of all reception data,

(b) a circuit for outputting the subtraction input value obtained in step (a) only for the data coinciding with the code pattern of segment synchronous signal, and

(c) a circuit for outputting said subtraction input value obtained in step (b) as a clock phase error signal only for the data positioned at the segment synchronous signal, wherein only the phase errors of a second symbol and a third symbol of said segment synchronous signal are outputted as said clock phase error.

7. (Cancelled)

8. (Previously presented) A digital broadcast demodulator of claim 2, being an apparatus for receiving digital broadcast by transmitting digital video and audio information coded by digital VSB modulation system in packet form,

wherein a synchronous signal in the received packet data is detected, the difference between the detected data value of the synchronous signal and a predetermined reference value is determined, and automatic gain control is performed on the basis of this difference,

said digital broadcast demodulator further comprising an AGC error detecting circuit for detecting a specific position of synchronous signal from the signal showing detection and establishment of synchronous signal in the reception data and the signal showing position of synchronous signal, and issuing the error of the synchronous signal at this specific position and the reference value as a control signal.

9. (Cancelled)

10. (Cancelled)

11. (Previously presented) A digital broadcast demodulator according to claim 2, wherein said polarity of the most significant bit (MSB) of the reception transport packet data is either positive or negative.